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DEVELOPMENT PROGRAM FOR 3.0KW INVERTER

Militarized Inverter for use with  
fuel cell or battery power plants

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Final Report

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes the design, construction and testing of a static Inverter rated at 3.0 kilowatts. Circuit techniques were evaluated to obtain desired results with considerations to cost, reliability, maintainability, weight, size and efficiency. The application of this portable, rugged Inverter is to replace mechan- ical alternating generators used in the field.		

## SUMMARY

The objective of this development program was to design, construct and test a static Inverter rated at 3.0 kilowatts (or 3.75KVA at 0.9PF lagging) supplying ac outputs operating at inputs of 35 to 60 VDC from low voltage fuel cells or batteries. The Inverter furnishes the following output voltage connections for 60 or 400 Hz operation:

- (a) Single phase, 2 wire, 120 VAC  
3 wire, 120 VAC or 240 VAC
- (b) Three phase, 4 wire, 120 VAC or 208 VAC.

Considerations for Inverter design included low production cost, reliability, maintainability, weight, size and efficiency. The Inverter basically consists of three separate 1 KW modules with one integral exhaust fan. Also included are three peripheral modules for bias, logic and EMI filtering.

## PREFACE

The program was authorized and controlled by the United States Army Mobility Equipment Research and Development Command. Contract DAAK70-77C-0012 was awarded to Gulton Industries, Incorporated, Engineered Magnetics Division, in October 1976 to perform the engineering task per Purchase Description EED 76 022501 to design 3.0 KW Silent Lightweight Electrical Energy Plant (SLEEP) Inverter. A prototype of the Inverter was fabricated and delivered, and will be used with fuel cells or battery power plants.

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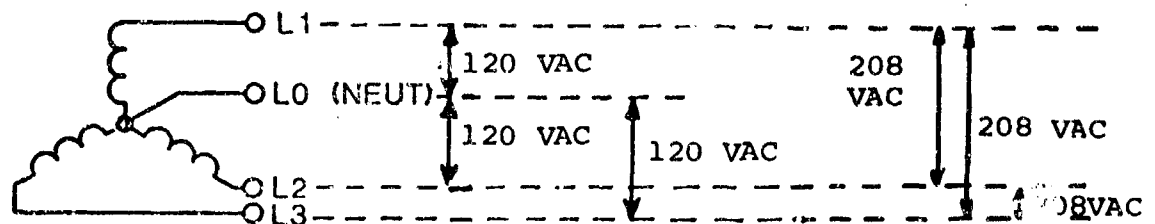
## INTRODUCTION

This report describes the program for the design, fabrication and testing of a 3 KW static Inverter. The program was conducted at Gulton Industries, Incorporated. Engineered Magnetics Division, as authorized and controlled by United States Army Mobility Equipment Research and Development Command Contract Number DAAK70-77C-0012, effective October, 1976. One prototype was built, tested and delivered, as required.

This militarized, modular Inverter, Gulton Model No. EMIR302, was designed per Purchase Description EED 76 022501 for a 3 KW Silent Lightweight Electrical Energy Plant (SLEEP) Inverter. The Inverter's 35-60 VDC input will be from a fuel cell or battery and supplies ac voltages at selectable 60 Hz or 400 Hz frequency with the following connections:

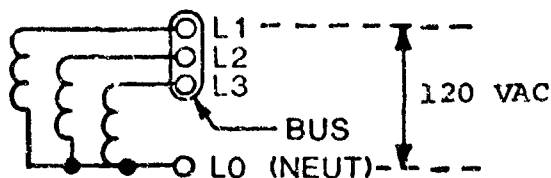
### 3Ø, 4 WIRE CONFIGURATION

120/208V-L1,L2,L3  
1.25 KVA, .8PF PER LINE



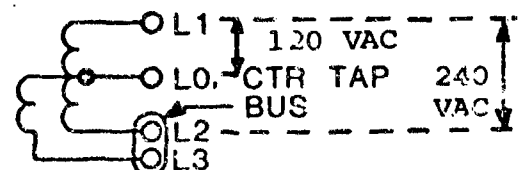
### 1Ø, 2 WIRE PARALLEL CONFIGURATION

120V-L1,L2,L3  
3.75 KVA, .8PF



### 1Ø, 3 WIRE CTR TAPPED CONFIGURATION

120/240V-L1,L2,L3  
1.25 KVA, .8PF PER LIN



The 60 or 400 Hz output with single phase 120/240 volts or three phase 120/208 volts can provide an input for the operation of most ac equipment. It is readily seen that the output can also be connected for two phase operation. Each phase, however connected, accommodates output power of 1 KW (or 1.25 KVA at 0.8 PF). The output voltage is a sinusoidal waveform.

Design consideration requirements and actual achievements as determined from the prototype are compared in Table 1.

TABLE 1. DESIGN CONSIDERATIONS

	Specification Requirement	Actual Achievement
Weight	110 lbs	125 lbs
Volume	2500 in. <sup>3</sup>	4626.4 in. <sup>3</sup>
Reliability (MTBF)	1200 hrs	7500 hrs**
Maintenance (MTTR)	1.5 hrs for Organizational, 6 hrs for higher echelons	Modular construction achieves this requirement.
Cost	-	
Efficiency*	85%	80 to 82%

\*Input voltage shall be between 40 and 60 VDC.

\*\*As calculated, see separate report, Gulton Report No. 2960 (February 2, 1979).

The electrical requirements of the Inverter are stated in Table 2. Inverter serial number 57812 performed well within the listed requirements when subjected to a test program prior to delivery. Typical test results are shown in Appendix I.

TABLE 2. ELECTRICAL REQUIREMENTS

Output Voltage Regulation	±2%
Output Frequency	$\left\{ \begin{array}{l} 60 \pm 0.3 \text{ Hz} \\ 400 \pm 2 \text{ Hz} \end{array} \right.$
Output Power	$\left\{ \begin{array}{l} 3 \text{ KW at } 1.0 \text{ PF} \\ \text{or} \\ 3.75 \text{ KVA at} \\ 0.8 \text{ PF lagging} \end{array} \right.$
Output Voltage Adjustment	±10%
Voltage Unbalance with Balanced Load	±10%
Voltage Unbalance with Unbalanced Load	±1%
Output Voltage Stability (30 seconds)	±1%
Output Voltage Stability (40 hours)	±2%
Output Frequency Stability (30 seconds)	±0.5%
Output Frequency Stability (4 hours)	±1%
Output Voltage Drift (60°F change) over 8 hours	±1%
Output Voltage Transients	
Application of Rated Load:	
Voltage Dip	20%
Voltage Recovery	3 sec
Rejection of Rated Load:	
Voltage Rise	30%
Voltage Recovery	3 sec
Output Frequency Transients	
Application of Rated Load:	
Undershoot	4%
Recovery	4 sec
Rejection of Rated Load:	
Overshoot	4%
Recovery	4 sec
Three Phase Output Waveform	
Maximum deviation factors	5%
Maximum single voltage harmonic	2%
Single Phase Output Waveform	
Maximum deviation factors	6%
Maximum single voltage harmonic	3%



## DISCUSSION

The design approach uses three identical single phase inverters, each supplying 1 KW of power. Each inverter is fabricated as a module and its single phases can be connected as: three phase, 4 wire, 120 VAC or 208 VAC; single phase, 2 wire, 120 vac; single phase, 3 wire, 120/240 VAC. Provisions are made on a panel to select the mode of operation. The output voltage is a sinusoidal waveform. Also, the frequency is selectable; 60 or 400 Hz. The modular construction of identical single phase inverters allows for low cost and easy replacement of an inoperable phase.

The initial design approach of the inverter module was to use a converter regulator circuit which would reduce parts and cost yet obtain high efficiency. After 4 months into the program, this approach was abandoned due to its inherent propensity to catastrophic failures if a control circuit did not function properly because of noise or other unexpected signals. Developing additional protective circuits to prevent the converter regulator from catastrophic power failures caused by extraneous sources would be time consuming, complicated and costly. Hence, a pulse width regulator and current driven DC to DC converter was used in the final configuration of the inverter module.

A complete single phase, 1 KW inverter module was tested for line and load regulation. See Tables 3 and 4 for test data. The tests were performed with the Bias Regulator and Converter module A5 and the Inverter Control Board (logic) module A4.

The block diagram of the inverter module is shown in detail as part of the overall diagram of the Static Inverter. See Figure 1.

A single Inverter Control Board (Logic) which replaced an earlier design of three independent logic control circuits (one in each 1 KW inverter module) was developed. This Inverter Control Board fulfills all the logic requirements for the three 1 KW inverter modules and eliminates the need of circulating logic signals between modules for the three-phase, single-phase and single-phase

TABLE 3. SINGLE PHASE, 1 KW INVERTER MODULE,  
LINE & LOAD REG TEST DATA AT 60 HZ

V <sub>IN</sub> DC	LOAD	V <sub>OUT</sub>	DISTORTION
60.0	OVA PF=1	120.50	1.75%
50.0		120.49	1.75%
40.0		120.49	1.75%
37.0		120.48	1.75%
60.0	272VA PF=1	120.37	1.85%
50.0		120.38	1.85%
40.0		120.36	1.85%
37.0		120.36	1.85%
60.0	544VA PF=1	120.31	1.90%
50.0		120.31	1.90%
40.0		120.29	1.90%
37.0		120.26	1.90%
60.0	816VA PF=1	120.24	1.95%
50.0		120.22	1.95%
40.0		120.17	1.95%
37.0		120.15	1.95%
60.0	1088VA PF=1	120.06	2.15%
50.0		120.00	2.15%
40.0		119.58	2.15%
37.0		119.04	2.15%

Data Regulation: +.42%, -.8%  
Spec Limit: ±2%

TABLE 4. SINGLE PHASE, 1 KW INVERTER MODULE,  
LINE & LOAD REG TEST DATA AT 400 HZ

V <sub>IN</sub> DC	LOAD	V <sub>OUT</sub>	DISTORTION
60.0	OVA PF=1	119.94	1.95%
50.0		119.92	1.95%
40.0		119.91	1.95%
37.0		119.91	1.95%
60.0	272VA PF=1	119.79	1.90%
50.0		119.79	1.90%
40.0		119.78	1.90%
37.0		119.78	1.90%
60.0	544VA PF=1	119.73	1.85%
50.0		119.73	1.85%
40.0		119.71	1.85%
37.0		119.68	1.85%
60.0	816VA PF=1	119.69	1.82%
50.0		119.69	1.82%
40.0		119.63	1.82%
37.0		119.61	1.82%
60.0	1088VA PF=1	119.60	1.90%
50.0		119.56	1.90%
40.0		119.45	1.90%
37.0		119.40	1.90%

Data Regulation: +.05%, -1%  
Spec Limit: ±2%

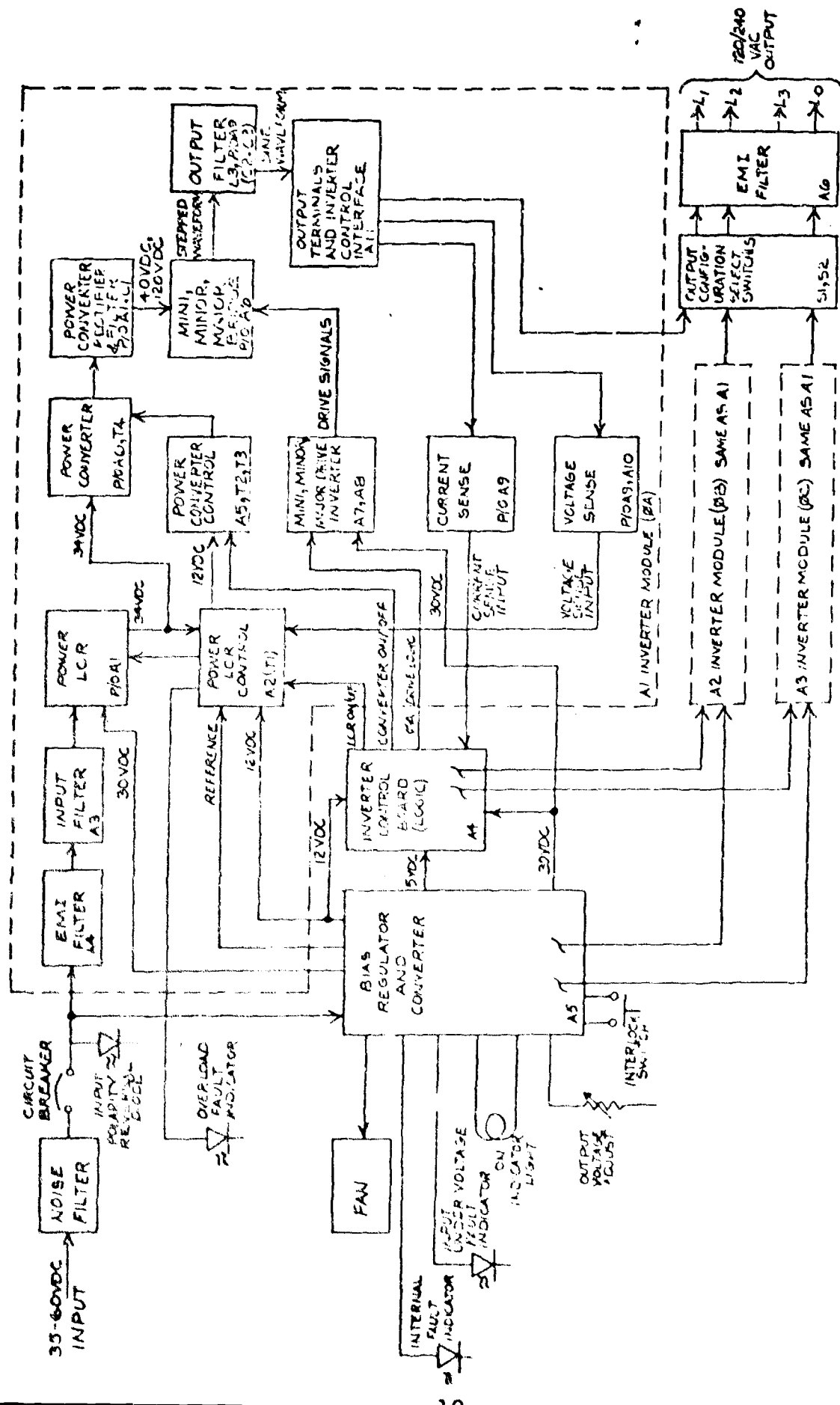


FIGURE 1 . INVERTER BLOCK DIAGRAM

center tap. In addition, operating all logic circuits on the same ground potential plane eliminated difficulties related to ground loops and noise. Furthermore, this circuit enables the output voltage connections to be selected using one four pole-three position switch as compared to two such switches required previously.

The Inverter is self-protected as required by the Purchase Specification for input polarity reversal, low input voltage, and output short circuit and overload. A diode serves as a protection against input polarity reversal by clamping the input voltage when reversed. Low input voltage ( $\leq 33$  VDC) and output overload for 30 seconds or longer (including short circuit) causes fault signal circuits to force the Inverter to turn off and remain in the off state until the input voltage is recycled. A light emitting diode (LED) illuminates providing visual indication for each of the input undervoltage and output overload fault condition. In addition, a similar sequence of unit turn off is effected when there is a failure in the bias regulator section of the Inverter. This is designated as an internal fault, also indicated by illumination of an LED, and was added to avoid unnecessary on-off recycling when the fault is other than low input voltage or overload. The unit is not electrically protected against high input since the unit will inherently operate at transient voltages of up to 100 VDC.

To avoid the effects of altitude, temperature, loads, aging and drift of the output frequency as produced by an alternating generator/inverter, this static Inverter utilizes a crystal controlled oscillator whose principal frequency is 2.16 MHz. The crystal is located on the Inverter Control Board A4. The 400 and 60 Hz frequency is locked to this stable frequency thereby eliminating all problems associated with frequency variations.

Leakage reactance in the major, minor and mini bridge drive transformers induced an undesirable output waveform phase shift; i.e., when the step waveforms of the three bridges are summed, the

steps failed to add and subtract in the proper sequence. Leakage reactance of the drive transformers were measured:

Major bridge transformer leakage: 21  $\mu\text{H}$

Minor bridge transformer leakage: 16  $\mu\text{H}$

Mini bridge transformer leakage : 13  $\mu\text{H}$

Using the circuit in Figure 2, waveform delays resulting from the leakage reactance were calculated using the circuit shown in Figure 3.

Major bridge waveform delay: 10.5  $\mu\text{S}$  at  $I_o = 1.5\text{A}$

Minor bridge waveform delay: 8  $\mu\text{S}$  at  $I_o = 1.5\text{A}$   
1.73  $\mu\text{S}$  at  $I_o = 0.4\text{A}$

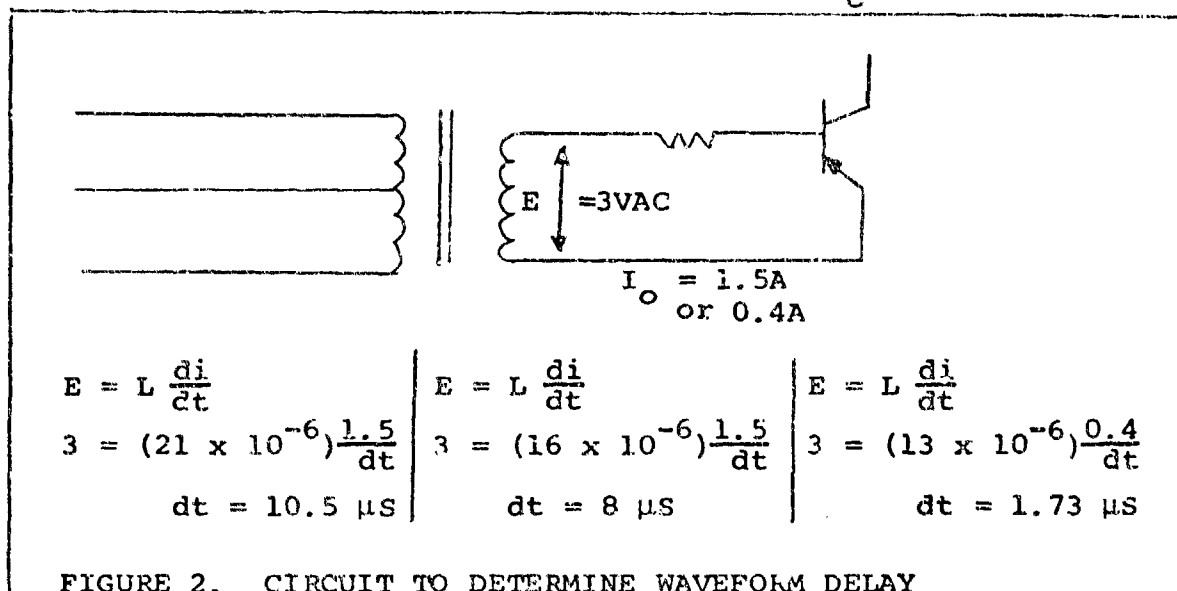


FIGURE 2. CIRCUIT TO DETERMINE WAVEFORM DELAY

At 60 Hz, an electrical degree is equal to 46  $\mu\text{S}$ . Therefore, the calculated delays at 60 Hz are insignificant. However, at 400 Hz the electrical degree is equal to 6.94  $\mu\text{S}$  and the calculated delays are quite significant and increase the harmonic distortion of the output waveforms. To overcome this difficulty the transformers were redesigned (increase size of transformer core) to balance the leakage reactance between windings. The penalty to do this was an increase in weight of approximately one pound. Other methods considered to reduce leakage reactance but were not suitable were:

1. Use Supermunder core material; weight is reduced but cost will increase by a factor of four.
2. Interlace transformer windings by layers; cost will increase appreciably.
3. Reduce drive current requirements of the output bridges by using Darlington transistors; electrically unfeasible with present Darlington transistors available.

To form the output sine wave, the stepped wave inverter approach was used. The first technique to form a smooth sine wave was to use a 26 step, half cycle waveform. This was previously accomplished in high power (15KW, 60Hz) inverters which required a 300  $\mu$ F capacitor and a 200  $\mu$ H inductor as an output filter. In a 1 KW inverter, the use of such a large capacitor resulted in decreased efficiency and increased cost and volume. Because of this, it was necessary to reduce the capacitance and increase the inductance to obtain an acceptable voltage waveform harmonic content. Since high inductance was forthwith considered for the output filter design, a simpler and less costly nine step, half cycle waveform (see Figure 3) circuit was designed and found to improve the smoothness of the sine wave. Testing proved the harmonic content was also within acceptable limits. Just as important, the inverter control board (logic) module A4 became one-third less complicated utilizing the nine step, half cycle waveform instead of the 26 step, half cycle waveform.

Thermal data was obtained by subjecting a 1 KW inverter module to four different methods of cooling. Seven thermocouples were placed on suspected hot components. The selected cooling method had results of:

- (1) input air temp of 27°C
- (2) output air temp of 32°C
- (3) hottest component temp of 44.5°C.

The final Inverter cooling method has a 400 Hz Rotron Spartan exhaust fan pulling air over the three 1 KW modules. Based on the low temperature results indicated above, the slight decrease of cooling over the two adjacent inverter modules would not significantly increase the temperature to cause heating problems (see Figure 4). In addition, a high temperature test (125°C) performed to the final packaged Inverter indicated no electrical out-of-spec limits.

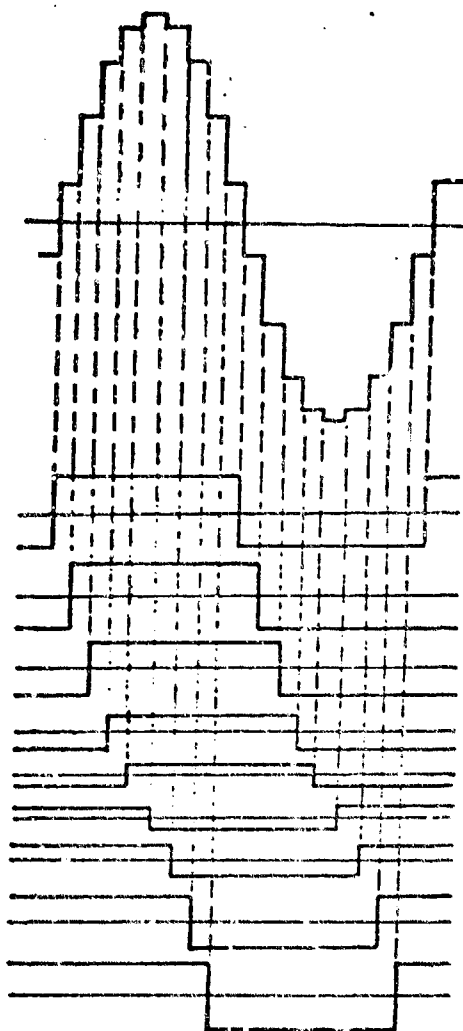


FIGURE 3. NINE STEP SINE WAVE



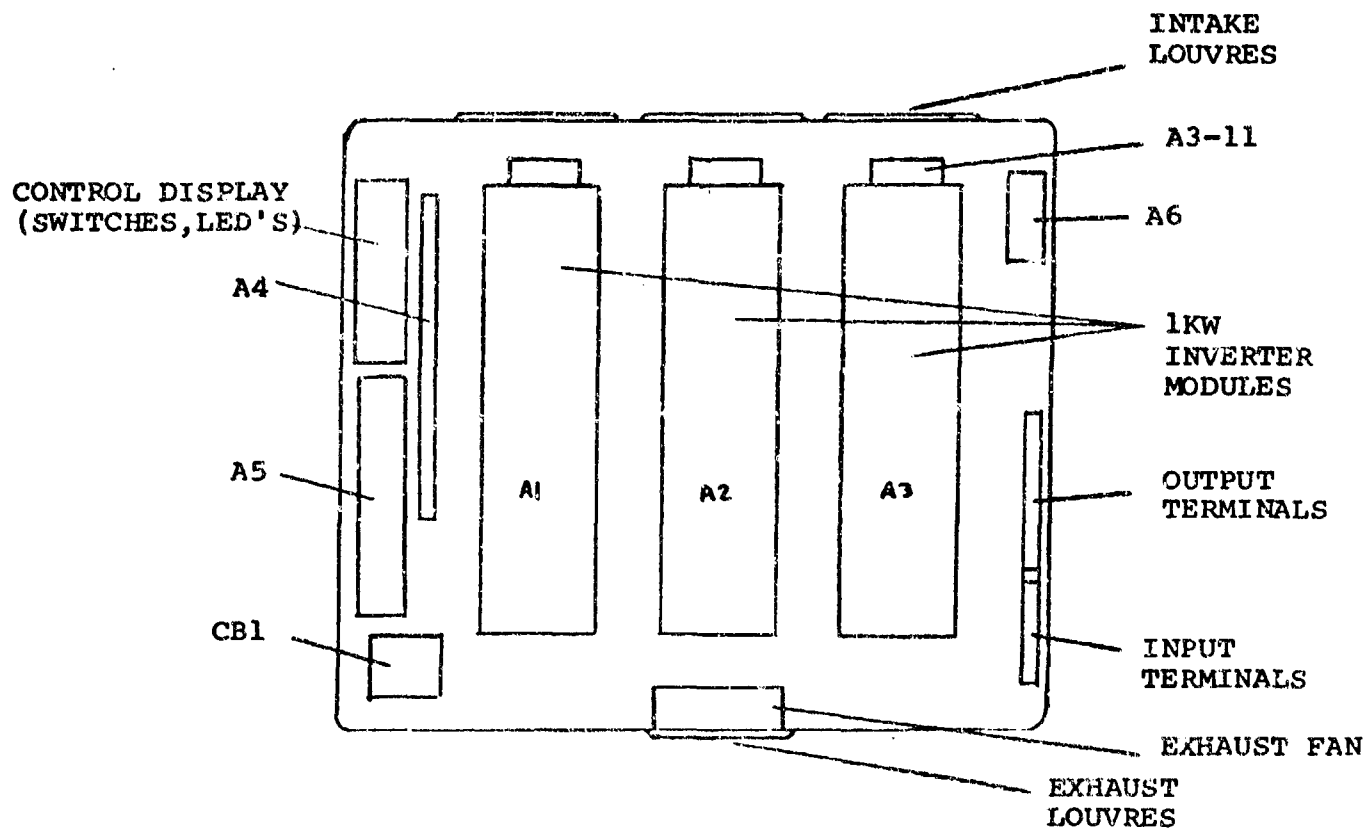


FIGURE 4. INVERTER LAYOUT (TOP VIEW)  
AND COOLING METHOD.

The early design of the 1 KW inverter module used three parallel sections in the power limit control regulator (LCR) which included three transistors procured from Solitron per Gulton Source Control Drawing 722770-1. To reduce cost, Solitron type SDT96303 transistors were inserted in place of the Gulton transistors and a comparison test of the power LCR circuit was performed. Results of this test are:

INPUT			OUTPUT			% EFF	TRANSISTORS USED
VDC	AMPS	WATTS	VDC	AMPS	WATTS		
60	40.8	2448	32.05	71.95	2306	94.2	Three SDT96303
60	40.9	2454	32.05	72.10	2311	94.17	Three 722770-1

From the data, it can be seen that the SDT96303 will replace the more expensive Gulton 722770-1 transistor (cost ratio 5:1) with no adverse effect on electrical operation. Also, the high current rating of the SDT96303 requires only a two section power LCR circuit needing two transistors connected in parallel to replace the three Gulton 722770-1 transistors previously used to share the power. This eliminates one section of the power LCR consisting of a choke, diode, capacitor and resistor, plus the driver circuit for the eliminated section consisting of a transistor, a diode and three resistors. The data below are the results of testing a complete 1 KW inverter module using the two section power LCR vs. the three section power LCR connected in parallel.

OUTPUT FREQUENCY AT 60 HZ					
INPUT			OUTPUT		
VDC	AMPS	WATTS	VAC	AMPS	WATTS
60.0	9.79	587.4	120.04	4.12	494.6
60.0	16.15	969.0	119.96	6.88	825.3
60.0	22.78	1366.8	119.83	9.60	1150.4
40.0	14.31	572.4	120.06	4.12	494.6
40.0	23.85	954.0	119.96	6.88	825.3
40.0	33.31	1332.4	119.71	9.60	1149.2
60.0	9.73	583.8	120.04	4.12	494.6
60.0	16.09	965.5	120.00	6.89	826.8
60.0	22.74	1364.4	119.88	9.60	1150.7
40.0	14.35	574.0	120.02	4.12	494.5
40.0	23.98	959.2	119.98	6.88	825.5
40.0	33.32	1332.8	119.75	9.60	1149.6

3 TRANSISTORS  
SDT96303

2 TRANSISTORS  
SDT96303

# OUTPUT FREQUENCY AT 400 HZ

INPUT			OUTPUT			
VDC	AMPS	WATTS	VAC	AMPS	WATTS	
60.0	9.66	579.6	119.55	4.10	490.2	3 TRANSISTORS SDT96303
60.0	15.96	597.6	119.50	6.82	814.9	
60.0	22.43	1345.8	119.44	9.53	1138.3	
40.0	14.09	563.6	119.52	4.10	490.0	
40.0	23.41	936.4	119.41	6.82	814.4	
40.0	32.88	1315.2	119.31	9.52	1135.8	
60.0	9.60	579.0	119.50	4.10	490.0	2 TRANSISTORS SDT96303
60.0	15.88	952.8	119.46	6.82	814.7	
60.0	22.39	1343.4	119.40	9.53	1137.9	
40.0	14.19	567.6	119.48	4.10	489.9	
40.0	23.50	940.0	119.45	6.82	814.6	
40.0	32.80	1312.0	119.30	9.52	1135.8	

In addition, power transistors in the power converter circuit and the minor and major bridge circuits use the Solitron SDT96303 to further reduce cost.

## CONCLUSIONS

The static Inverter electrical and mechanical design was established with no major difficulties. The weight specification requirement of 110 lbs was exceeded by 15 lbs which is an insignificant 13.5% increase considering that the unit application is to accompany battery power plants and is for ground field use. The Inverter operates with little noise and is lightweight compared to the alternating generators presently used in the field. The electrical design and component parts used is of the latest state-of-the-art technology for an Inverter with a highly regulated sine wave output.

The Inverter is modular constructed to facilitate maintainability and repair, and to minimize down-time.

The output power rating in conjunction with the Inverter size, weight and efficiency, plus the capability of single phase or three phase output voltage connections, augments the versatility of the Inverter.

#### RECOMMENDATIONS

Further effort can be expended to improve the mechanical packaging design to reduce cost. This can be accomplished using a cast housing which would also increase the overall Inverter weight. However, the trade-off of increase weight to decrease cost is tolerable with regard to unit application and transportability.

Allow for additional study to possibly replace discrete circuits with integrated circuits to reduce both cost and weight.

**APPENDIX I**

Typical test results of delivered Inverter (Ser. No. 57812) at worst case conditions (40 VDC input with output at full load):

Output Voltage Regulation:

3 $\phi$ , 4 wire; 60Hz	{ L1 120.1VAC L2 120.1VAC L3 120.5VAC
1 $\phi$ , 2 wire; 60Hz	119.9VAC
3 $\phi$ , 4 wire; 400Hz	{ L1 120.0VAC L2 120.0VAC L3 120.1VAC
1 $\phi$ , 2 wire; 400Hz	119.5VAC

Output Frequency:

3 $\phi$ , 4 wire	{ 59.99Hz 400.00Hz
1 $\phi$ , 3 wire	{ 59.99Hz 400.01Hz
1 $\phi$ , 2 wire	{ 60.00Hz 400.01Hz

Output Power:

	<u>Resistive</u>	<u>Inductive</u>
3 $\phi$ , 4 wire; 60Hz	{ L1 1012.4W L2 1018.4W L3 1007.4W	1214.3VA 1209.9VA 1218.2VA
1 $\phi$ , 2 wire; 60Hz	3013.1W	3626.7VA
3 $\phi$ , 4 wire; 400Hz	{ L1 999.6W L2 1009.2W L3 992.0W	1173.0VA 1158.5VA 1174.9VA
1 $\phi$ , 2 wire; 400Hz	2969.6W	3462.1VA

Output Voltage Adjustment: Adjusts to greater than 10% from nominal  $V_{OUT}$  for all conditions.

Voltage Unbalance with Unbalanced Load:

3 $\phi$ , 4 wire; 60Hz	{ Less than 1% deviation of $V_{OUT}$ when one phase is at no load, other phases at rated load.
3 $\phi$ , 4 wire; 400Hz	

Output Voltage Stability (40 seconds) 1 $\phi$ , 2 wire: 119.9VAC, No drift

Output Voltage Stability (2 hours) 1 $\phi$ , 2 wire: 120.0VAC, No drift

Output Frequency Stability (40 seconds) 1 $\phi$ , 2 wire: 60.03Hz, No drift

Output Frequency Stability (2 hours) 1 $\phi$ , 2 wire: 60.03Hz, No drift

Output Voltage Drift (60°F change, over 2 hours)

1Ø, 2 wire:

119.9VAC, No drift\*

Output Frequency Drift (60°F change, over 2 hours)

1Ø, 2 wire:

400.07 to 400.11 Hz\*

Output Voltage Transients

Application of Rated Load:		<u>60.03Hz</u>	<u>399.93Hz</u>
Voltage Dip	} 3Ø, 4 wire	10.7%	10.6%*
Voltage Recovery		0.3sec	0.3sec*
Voltage Dip	} 1Ø, 2 wire	10.7%	10.6%*
Voltage Recovery		0.3sec	0.3sec*
Rejection of Rated Load:			
Voltage Dip	} 3Ø, 4 wire	11.7%	12.1%*
Voltage Recovery		1.4sec	1.7sec*
Voltage Dip	} 1Ø, 4 wire	11.7%	12.1%*
Voltage Recovery		1.4sec	2.5sec*

Output Frequency Transients

Application of Rated Load:		<u>60.02Hz</u>	<u>400.16Hz</u>
Undershoot	} 1Ø, 2 wire	0.05%	0.06%*
Recovery		<0.15sec	<0.15sec*
Rejection of Rated Load:		<u>59.99Hz</u>	<u>399.93Hz</u>
Overshoot	} 1Ø, 2 wire	0.05%	0.06%*
Recovery		<0.15sec	<0.15sec*

Single Phase Output Waveform:		<u>60Hz</u>	<u>400Hz</u>
Maximum deviation factors		2.35%	2.10%
Maximum single voltage harmonic		1.98%**	1.8%**

\*\* at 17th harmonic

\* Data recorded during high temperature test (125°F).